FIG. 1

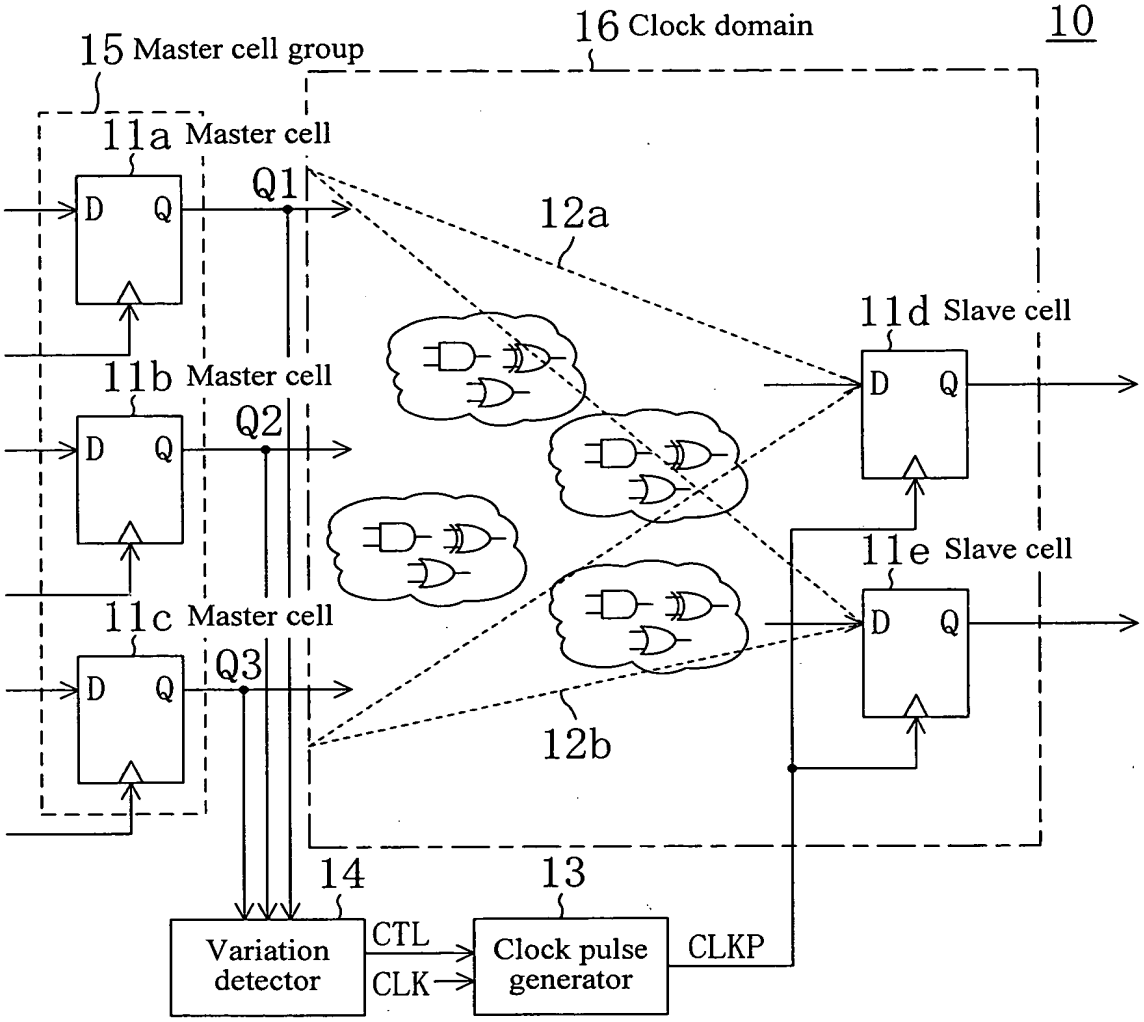
15 Master cell group
16 Clock domain
10
11a Master cell
Q1
12a
11d Slave cell
11b Master cell
Q2
11e Slave cell
11c Master cell
Q3
12b
14
13
Variation detector
CTL
CLK
Clock pulse generator
CLKP
D
Q

FIG. 2

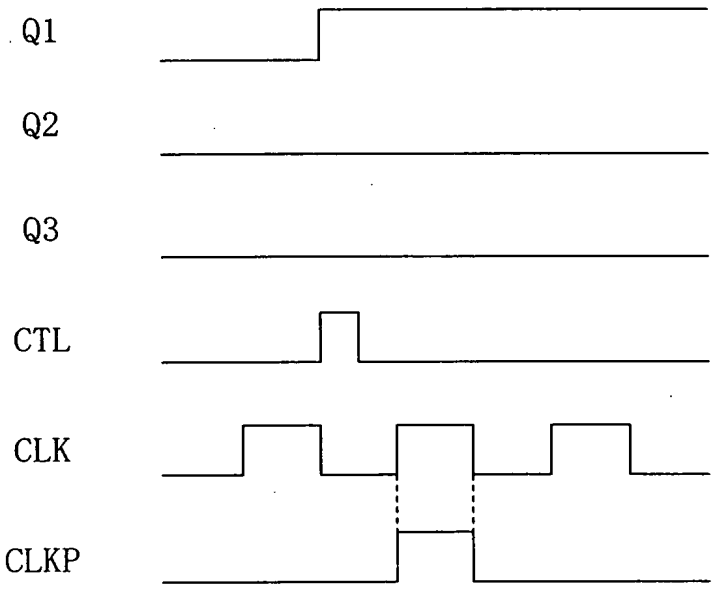

FIG. 3

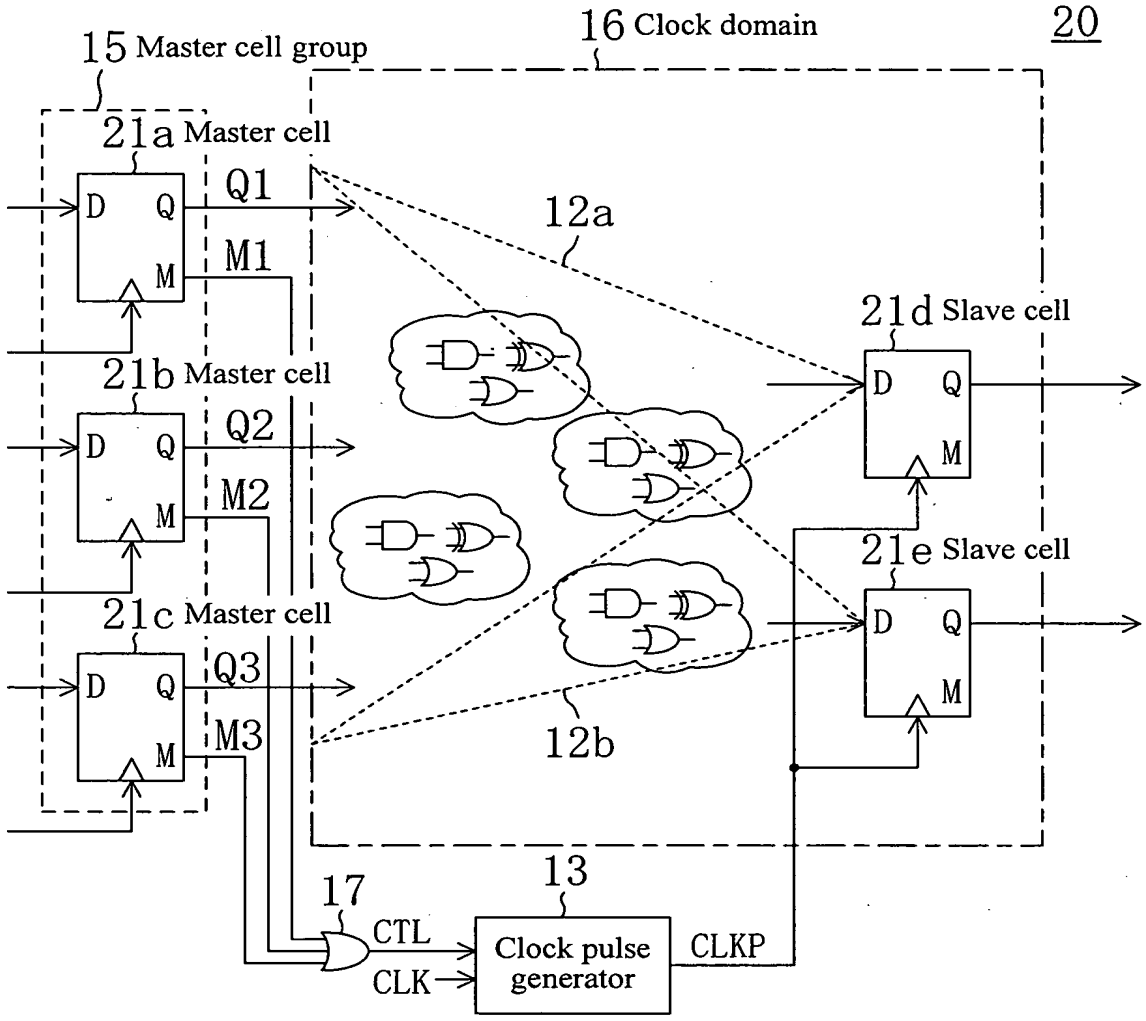
15 Master cell group
16 Clock domain
20
21a Master cell
21b Master cell
21c Master cell
21d Slave cell
21e Slave cell
D
Q
M
Q1
Q2
Q3
M1
M2
M3
12a
12b
13
17
CTL
CLK
Clock pulse generator
CLKP

FIG. 4

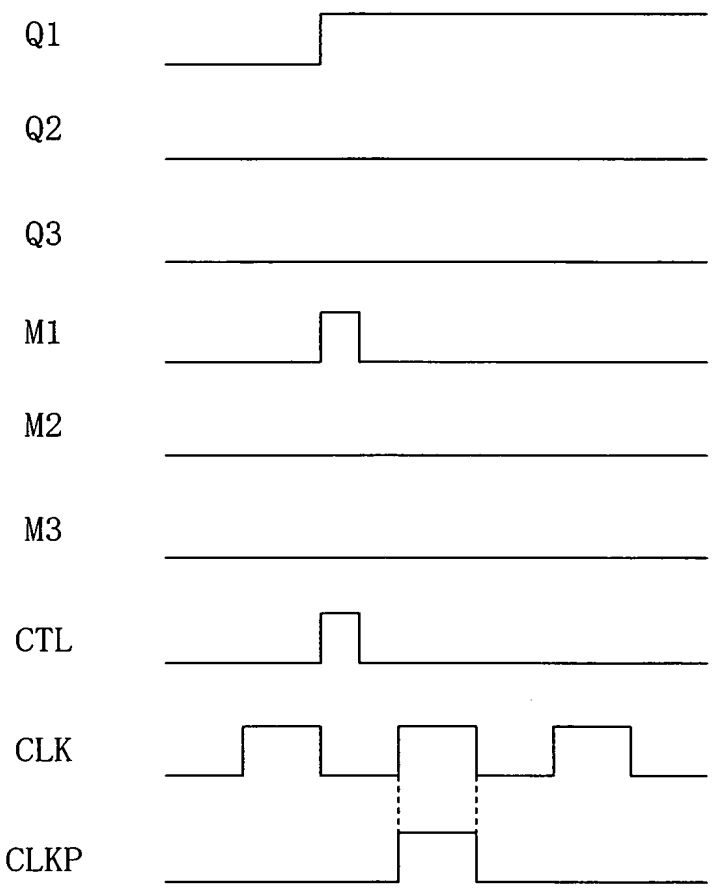

FIG. 5

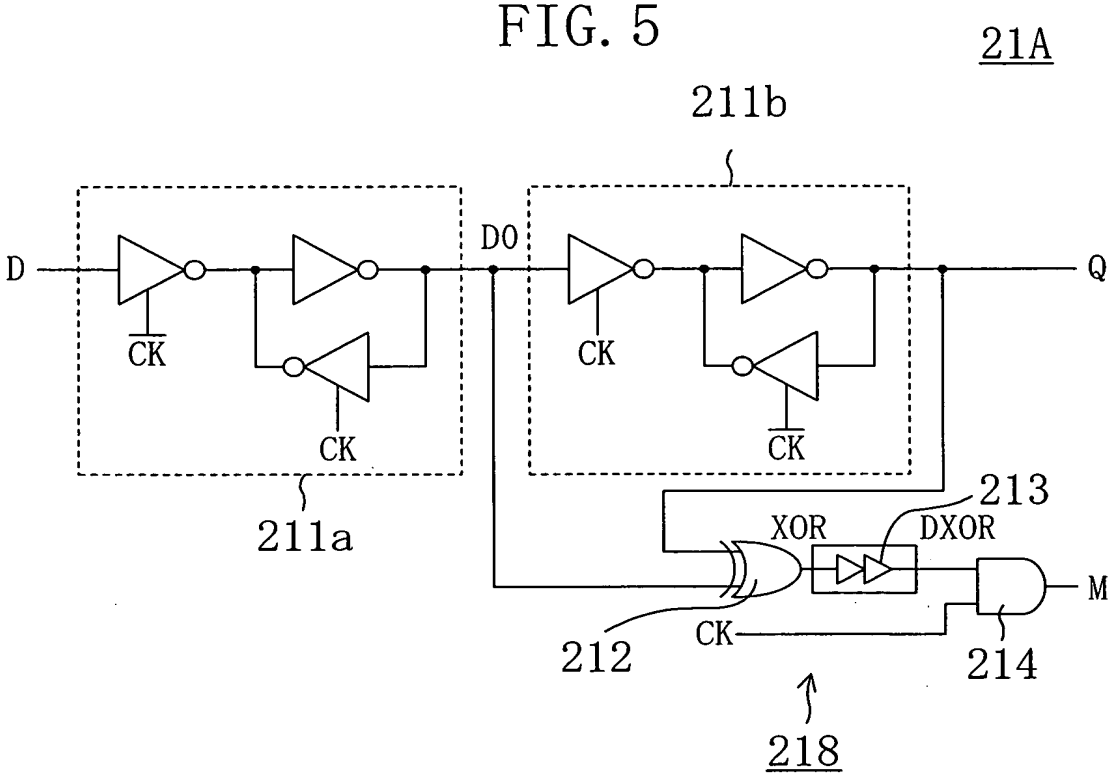
21A
211b
D
DO
Q
CK
CK
CK
CK
211a
213
XOR
DXOR
M
212
CK
214
218

FIG. 6

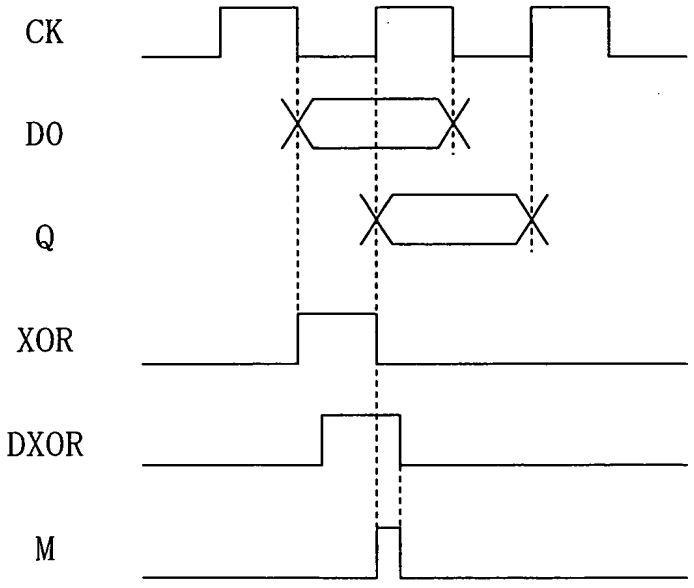
CK
DO
Q
XOR
DXOR
M

FIG. 7

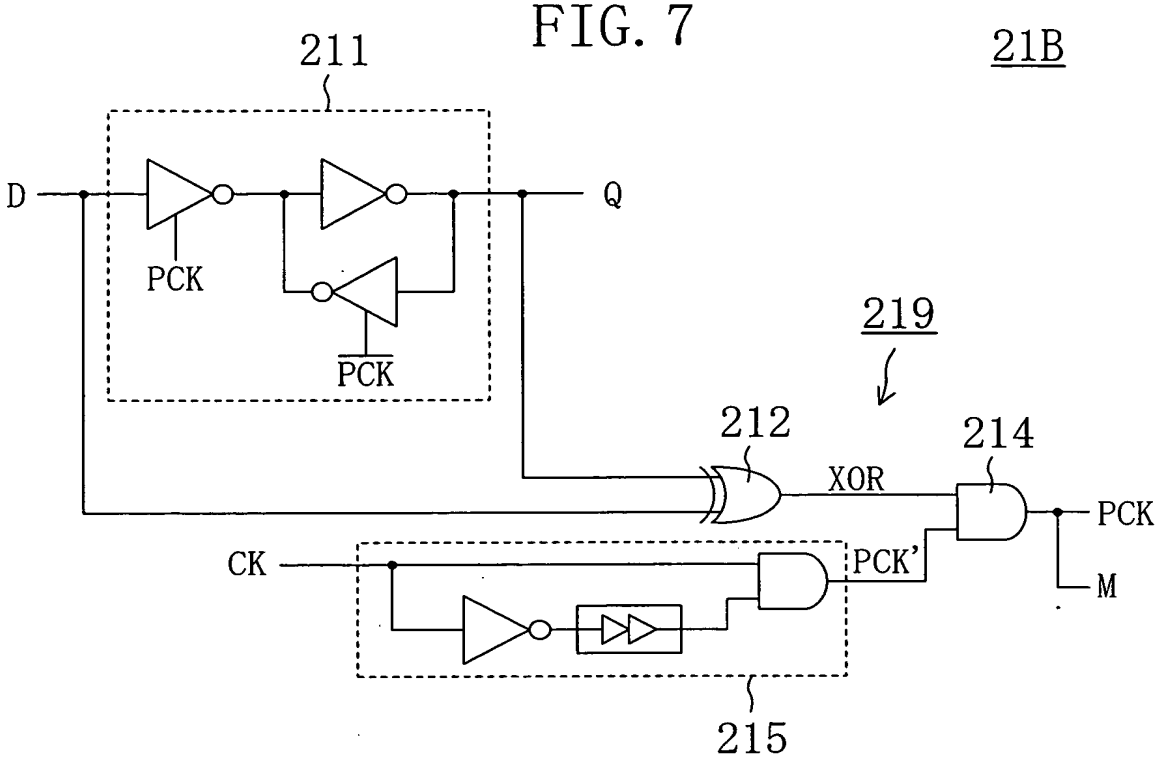
21B
211
D
Q
PCK
PCK
219
212
214
XOR
PCK
CK
PCK'
M
215

FIG. 8

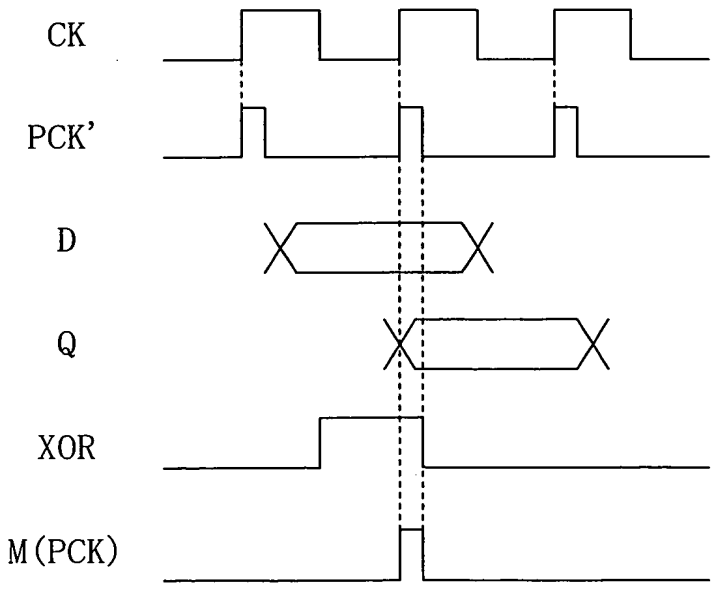
CK
PCK'
D
Q
XOR
M(PCK)

FIG. 9

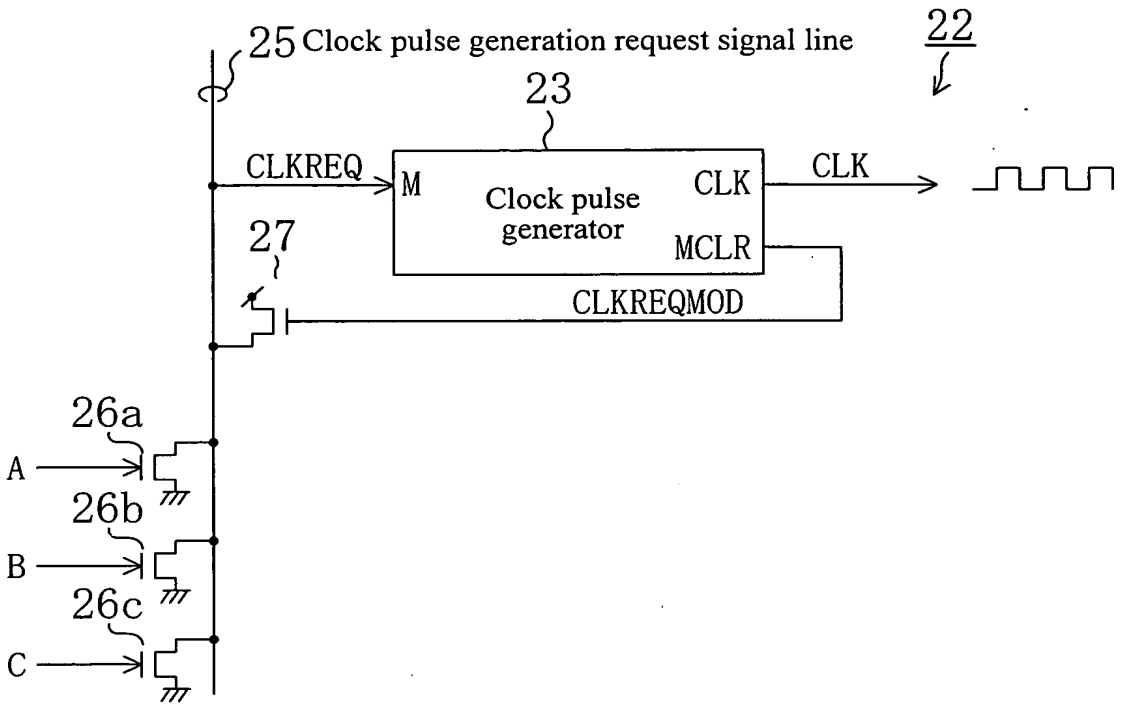
25 Clock pulse generation request signal line
22
23
CLKREQ
M
Clock pulse generator
CLK
CLK
MCLR
27
CLKREQMOD
26a
A
26b
B
26c
C

FIG. 10

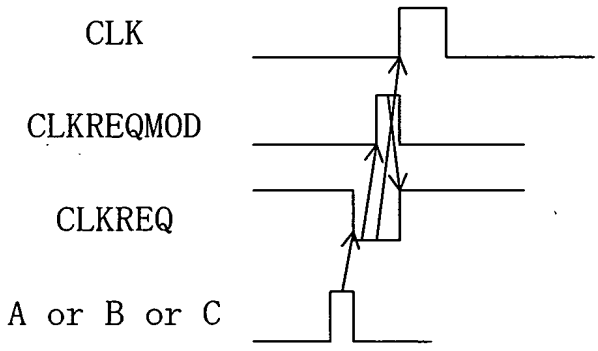
CLK
CLKREQMOD
CLKREQ
A or B or C

FIG. 11

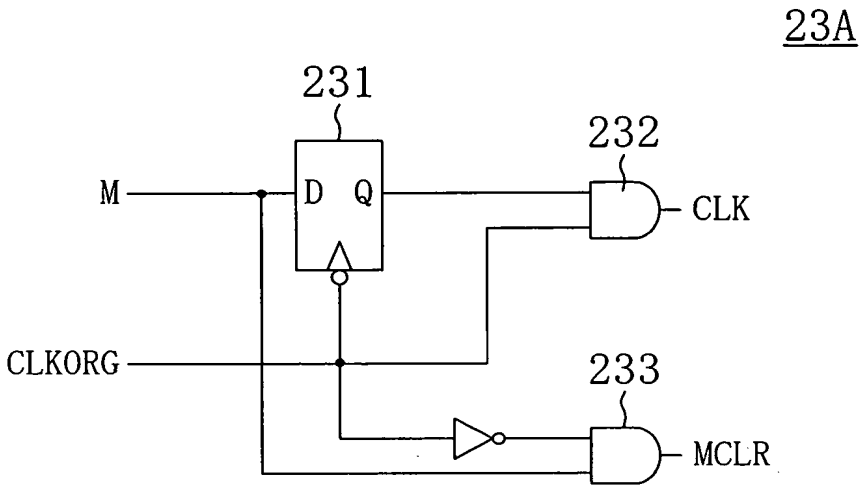

FIG. 12

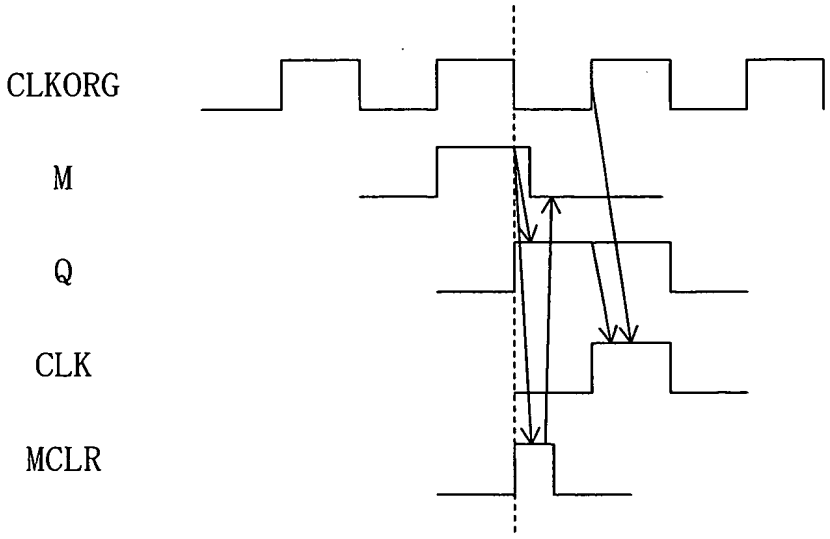

FIG. 13

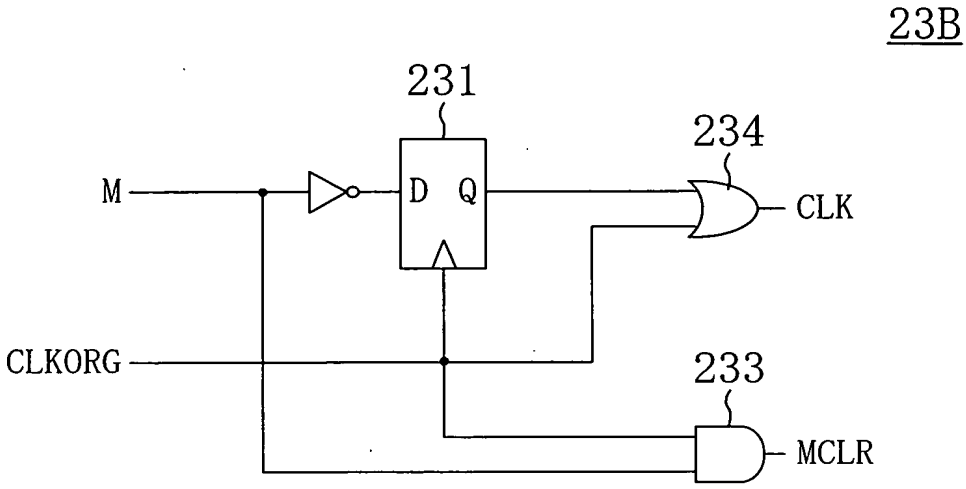

FIG. 14

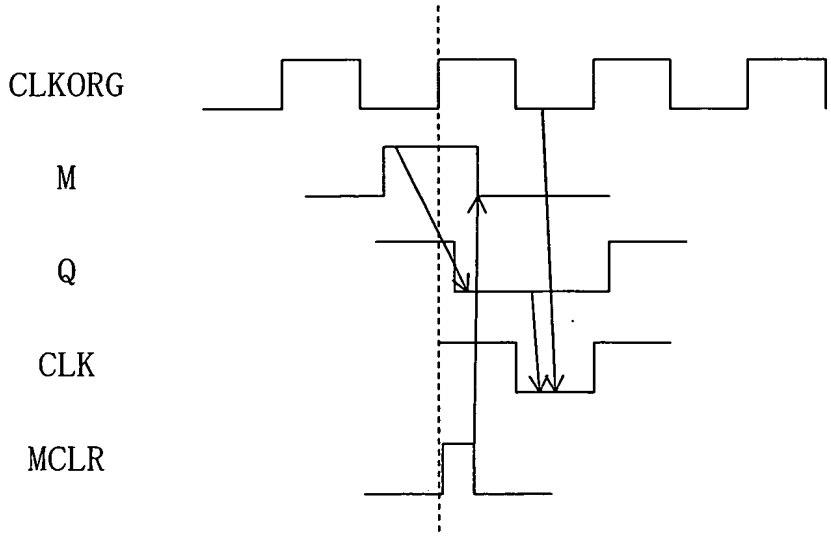

FIG. 15

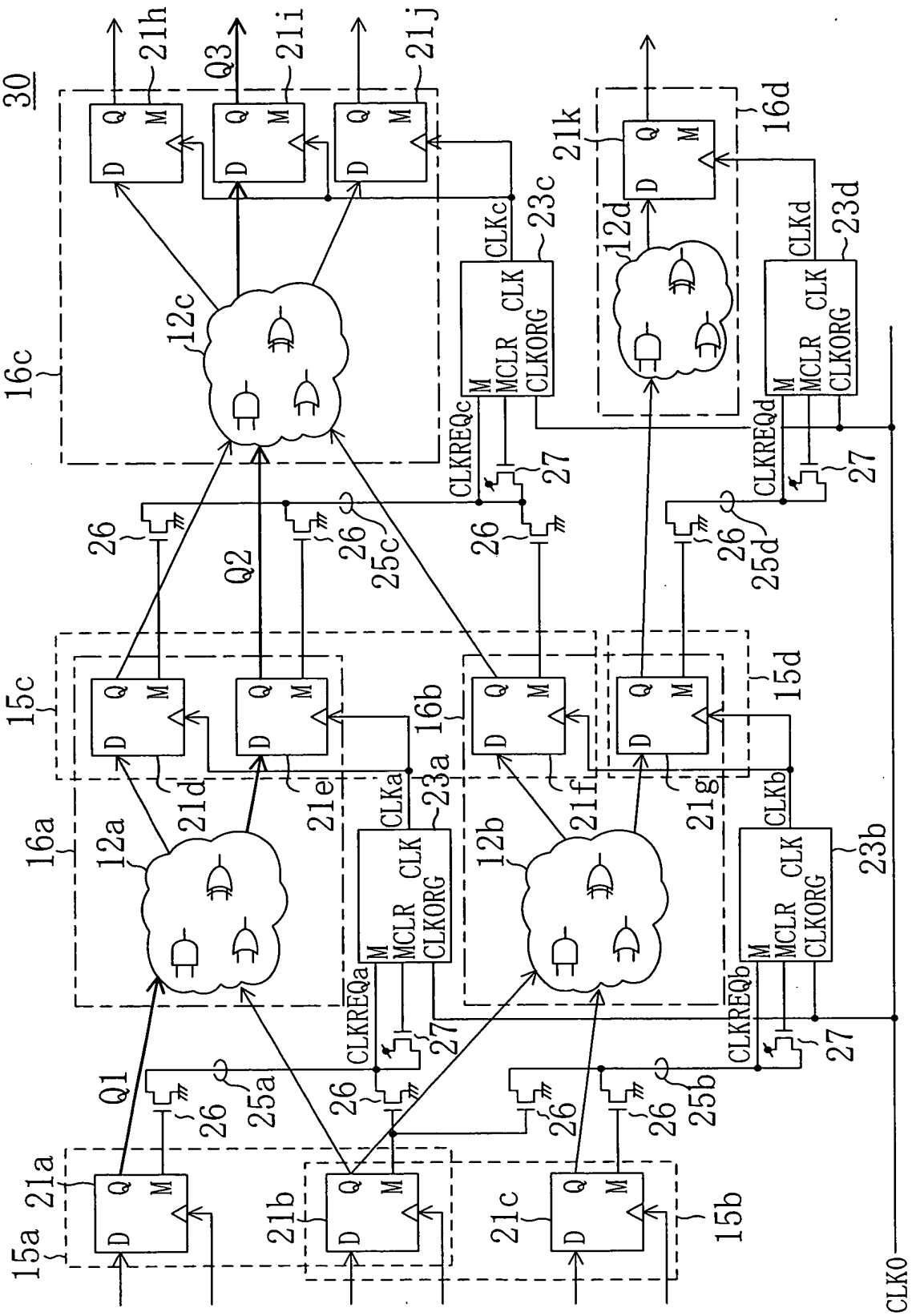
30
16c
16a
16b
16d
15a
15b
15c
15d
21a
21b
21c
21d
21e
21f
21g
21h
21i
21j
21k
12a
12b
12c
12d
23a
23b
23c
23d
CLKa
CLKb
CLKc
CLKd
CLKREQa
CLKREQb
CLKREQc
CLKREQd
MCLR
CLKORG
CLK
Q1
Q2
Q3
25a
25b
25c
25d
26
27
CLK0

FIG. 16

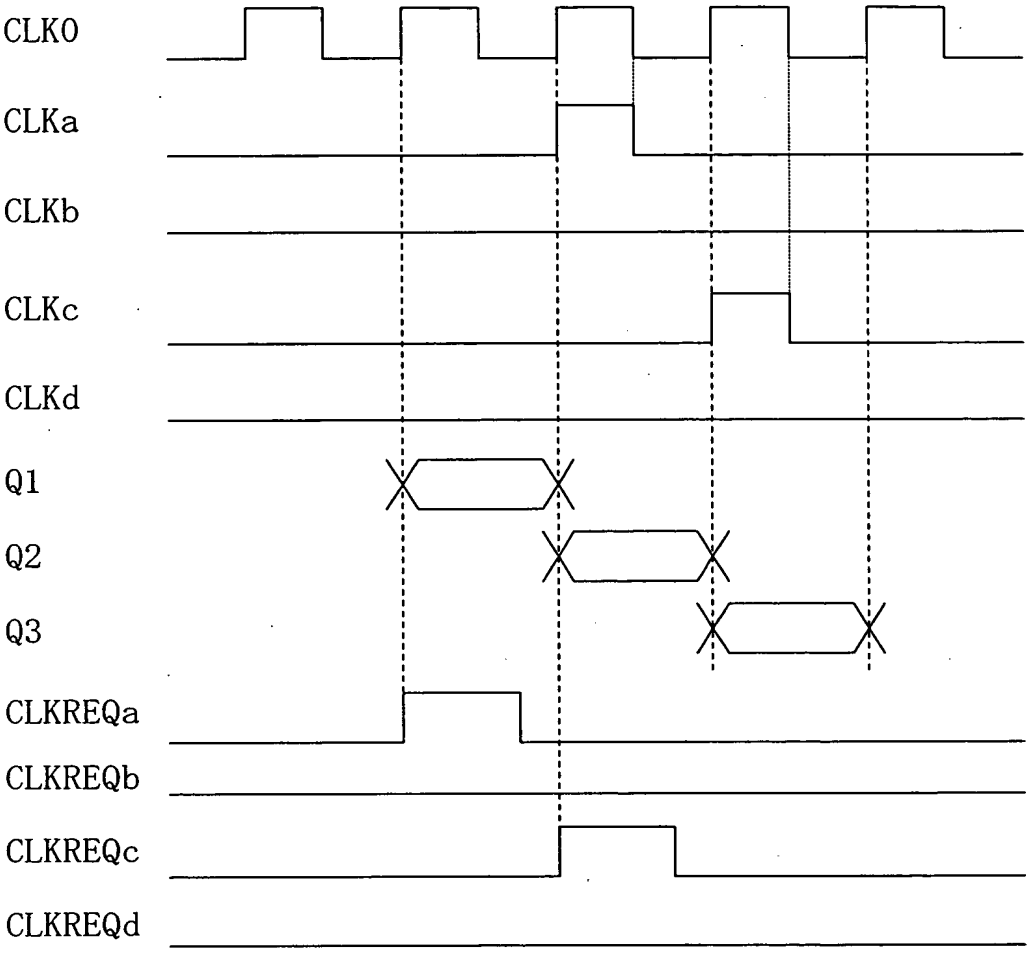
CLK0
CLKa
CLKb
CLKc
CLKd
Q1
Q2
Q3
CLKREQa
CLKREQb
CLKREQc
CLKREQd

FIG. 17

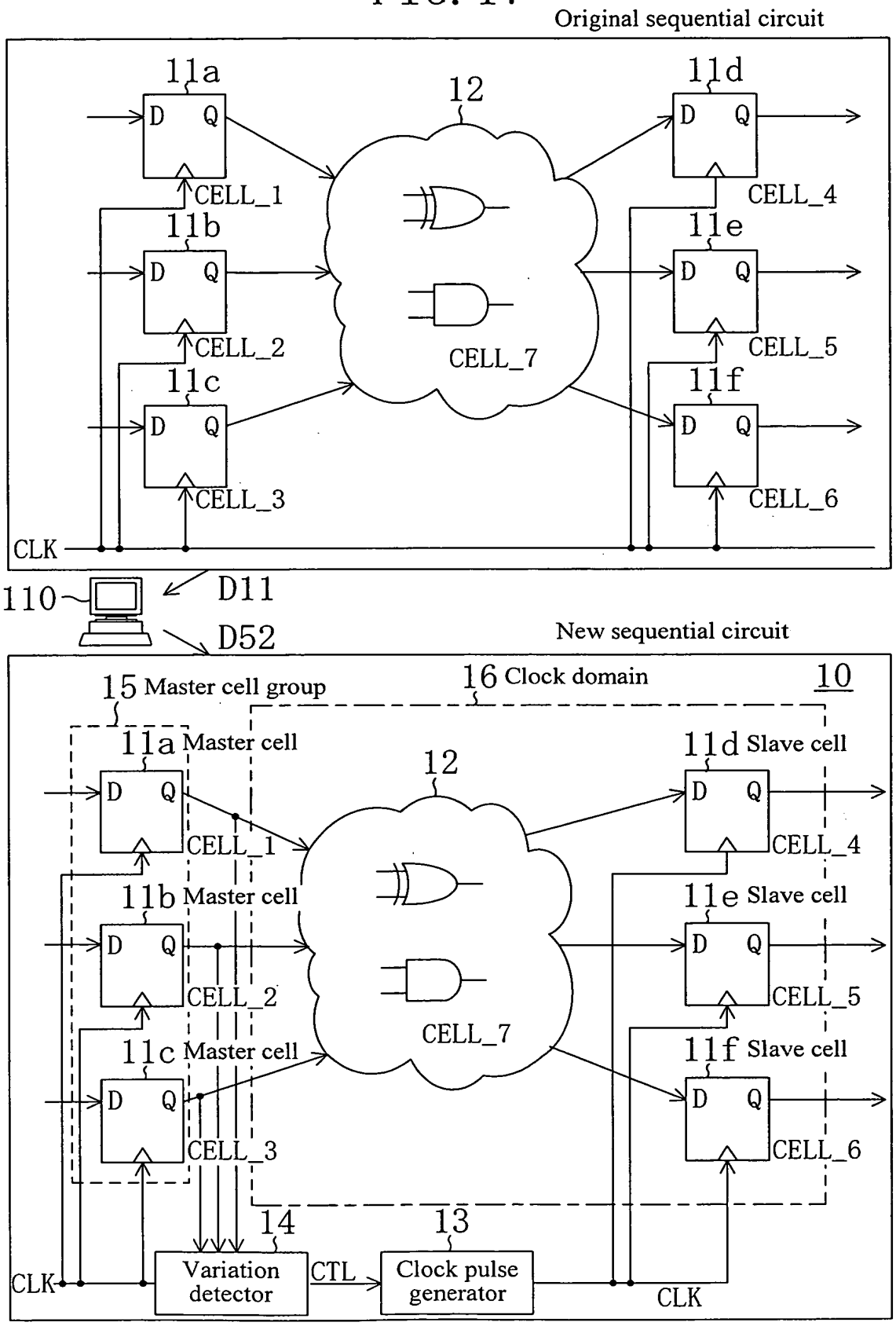
Original sequential circuit
11a
12
11d
D Q
CELL_1
CELL_4
11b
11e
CELL_2
CELL_5
CELL_7
11c
11f
CELL_3
CELL_6
CLK
110
D11
D52
New sequential circuit
15 Master cell group
16 Clock domain
10
11a Master cell
11d Slave cell
11b Master cell
11e Slave cell
11c Master cell
11f Slave cell
14
13
Variation detector
CTL
Clock pulse generator

FIG. 18

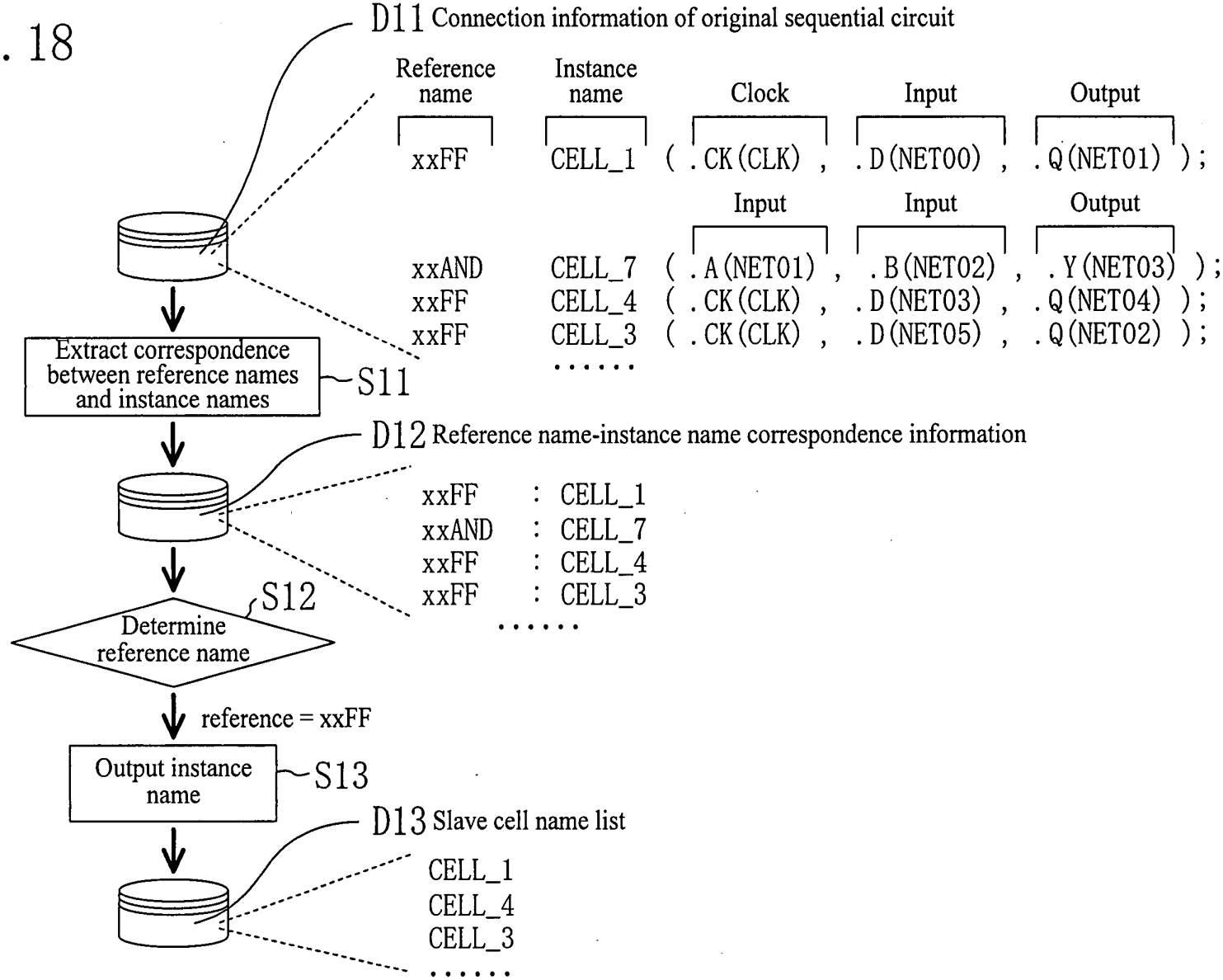
D11 Connection information of original sequential circuit
Reference name
Instance name
Clock
Input
Output
xxFF CELL_1 (.CK(CLK) , .D(NET00) , .Q(NET01));
Input
Input
Output
xxAND CELL_7 (.A(NET01) , .B(NET02) , .Y(NET03));
xxFF CELL_4 (.CK(CLK) , .D(NET03) , .Q(NET04));
xxFF CELL_3 (.CK(CLK) , .D(NET05) , .Q(NET02));
.....
Extract correspondence between reference names and instance names
S11
D12 Reference name-instance name correspondence information
xxFF : CELL_1
xxAND : CELL_7
xxFF : CELL_4
xxFF : CELL_3
.....
S12
Determine reference name
reference = xxFF
Output instance name
S13
D13 Slave cell name list
CELL_1
CELL_4
CELL_3
.....

FIG. 19

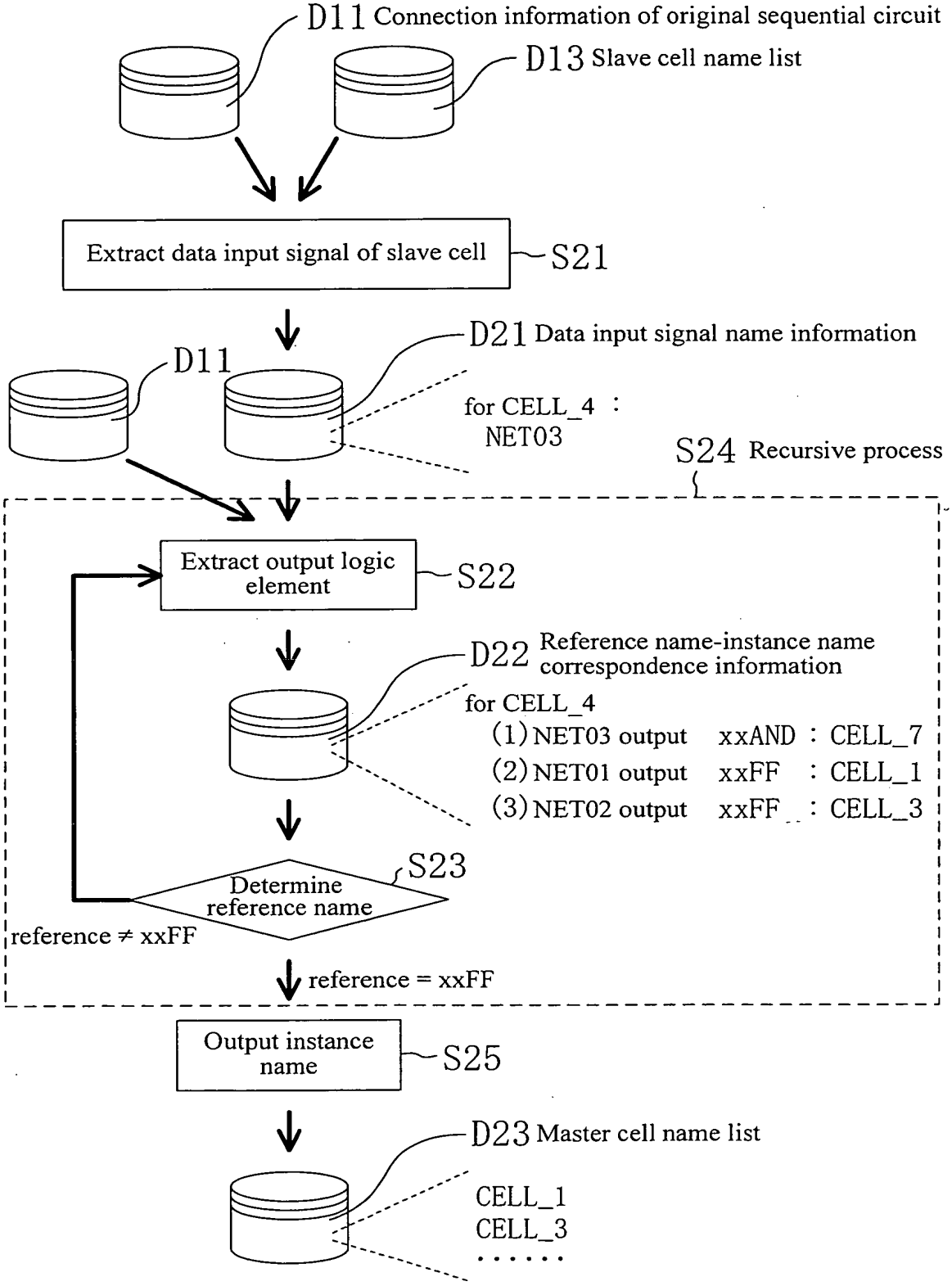
D11 Connection information of original sequential circuit
D13 Slave cell name list
Extract data input signal of slave cell
S21
D11
D21 Data input signal name information
for CELL_4 :
NET03
S24 Recursive process
Extract output logic element
S22
D22 Reference name-instance name correspondence information
for CELL_4
(1) NET03 output xxAND : CELL_7
(2) NET01 output xxFF : CELL_1
(3) NET02 output xxFF : CELL_3
S23
Determine reference name
reference ≠ xxFF
reference = xxFF
Output instance name
S25
D23 Master cell name list
CELL_1
CELL_3
.....

FIG. 20

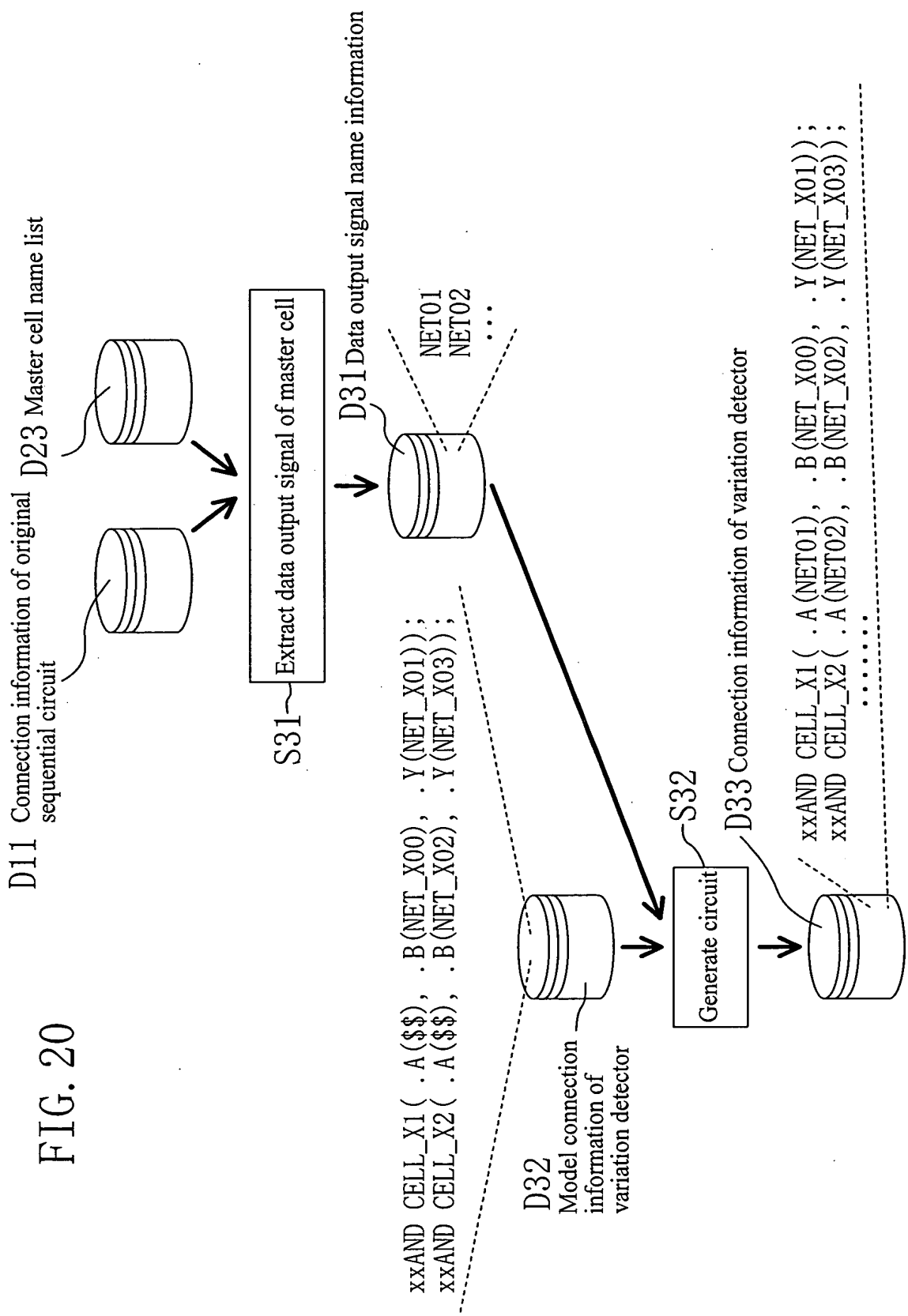
D11 Connection information of original sequential circuit
D23 Master cell name list
S31
Extract data output signal of master cell
D31 Data output signal name information
NET01
NET02
...
xxAND CELL_X1(.A($$), .B(NET_X00), .Y(NET_X01));
xxAND CELL_X2(.A($$), .B(NET_X02), .Y(NET_X03));
D32
Model connection information of variation detector
S32
Generate circuit
D33 Connection information of variation detector
xxAND CELL_X1(.A(NET01), .B(NET_X00), .Y(NET_X01));
xxAND CELL_X2(.A(NET02), .B(NET_X02), .Y(NET_X03));
.....

FIG. 21

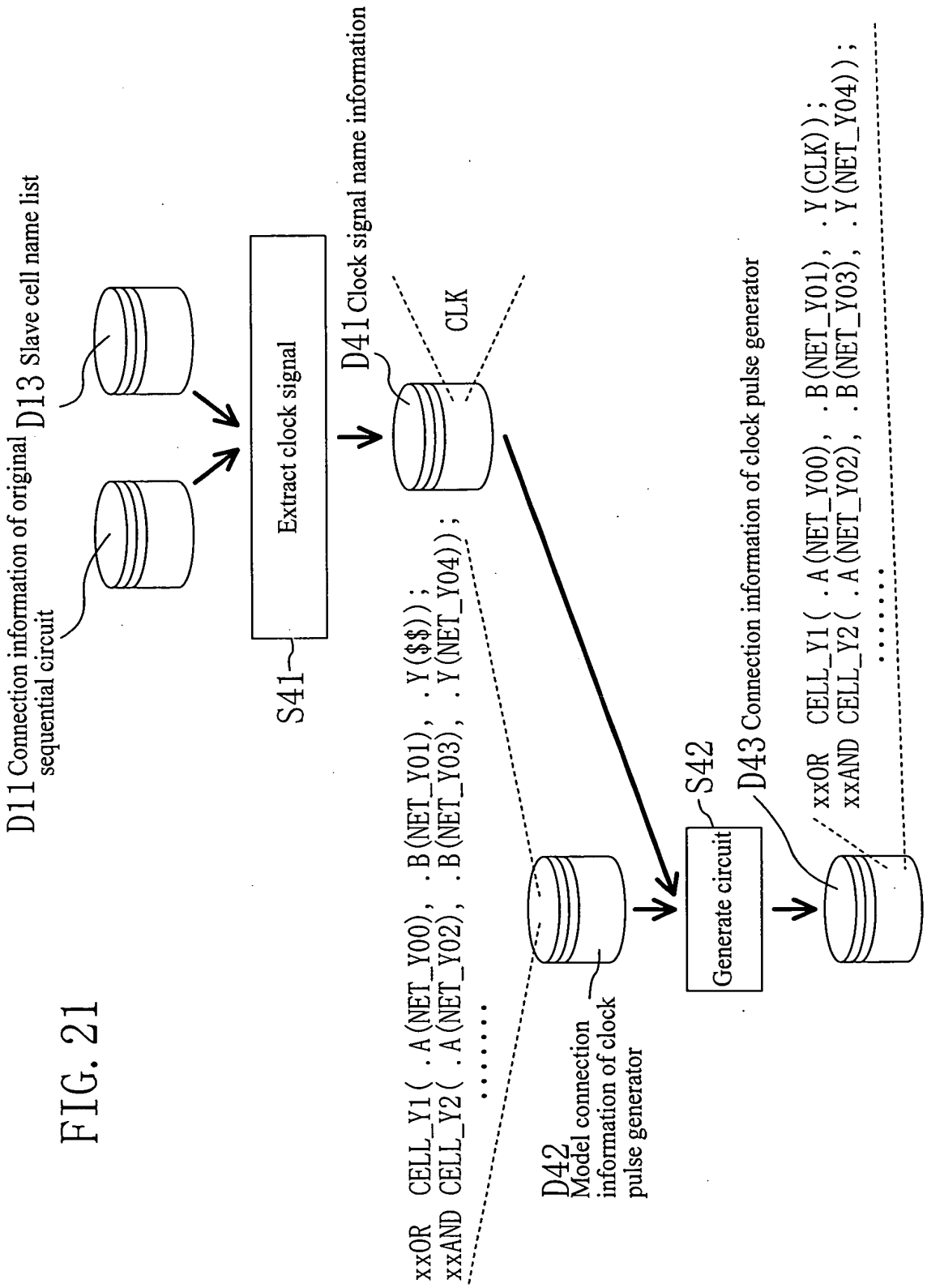
D11 Connection information of original sequential circuit
D13 Slave cell name list
Extract clock signal
S41
D41 Clock signal name information
CLK
xxOR CELL_Y1(.A(NET_Y00), .B(NET_Y01), .Y($$));
xxAND CELL_Y2(.A(NET_Y02), .B(NET_Y03), .Y(NET_Y04));
.....
D42 Model connection information of clock pulse generator
Generate circuit
S42
D43 Connection information of clock pulse generator
xxOR CELL_Y1(.A(NET_Y00), .B(NET_Y01), .Y(CLK));
xxAND CELL_Y2(.A(NET_Y02), .B(NET_Y03), .Y(NET_Y04));
.....

FIG. 22

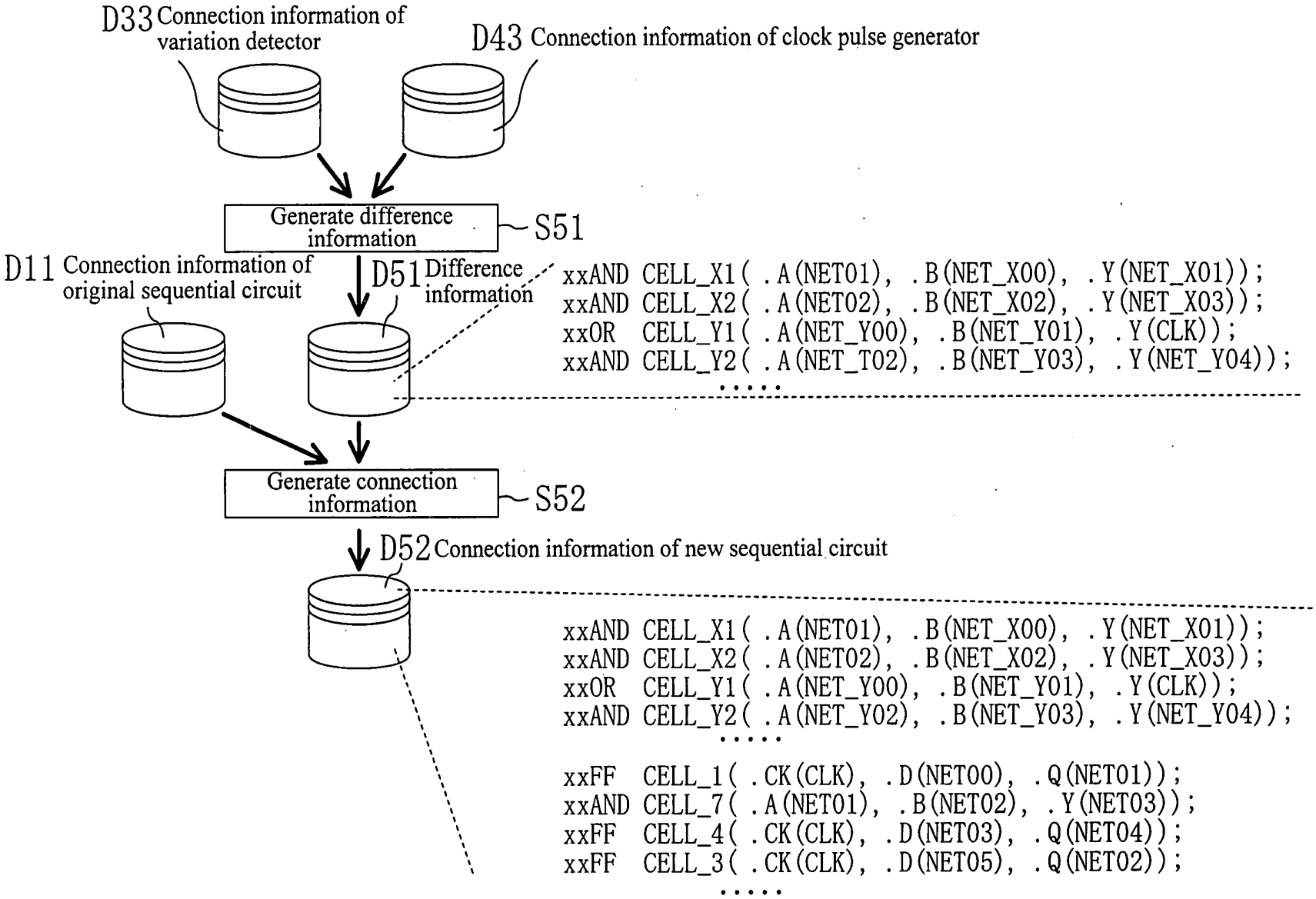
D33 Connection information of variation detector
D43 Connection information of clock pulse generator
Generate difference information
S51
D11 Connection information of original sequential circuit
D51 Difference information
xxAND CELL_X1(.A(NET01), .B(NET_X00), .Y(NET_X01));
xxAND CELL_X2(.A(NET02), .B(NET_X02), .Y(NET_X03));
xxOR CELL_Y1(.A(NET_Y00), .B(NET_Y01), .Y(CLK));
xxAND CELL_Y2(.A(NET_T02), .B(NET_Y03), .Y(NET_Y04));
.....
Generate connection information
S52
D52 Connection information of new sequential circuit
xxAND CELL_X1(.A(NET01), .B(NET_X00), .Y(NET_X01));
xxAND CELL_X2(.A(NET02), .B(NET_X02), .Y(NET_X03));
xxOR CELL_Y1(.A(NET_Y00), .B(NET_Y01), .Y(CLK));
xxAND CELL_Y2(.A(NET_Y02), .B(NET_Y03), .Y(NET_Y04));
.....
xxFF CELL_1(.CK(CLK), .D(NET00), .Q(NET01));
xxAND CELL_7(.A(NET01), .B(NET02), .Y(NET03));
xxFF CELL_4(.CK(CLK), .D(NET03), .Q(NET04));
xxFF CELL_3(.CK(CLK), .D(NET05), .Q(NET02));
.....

FIG. 23

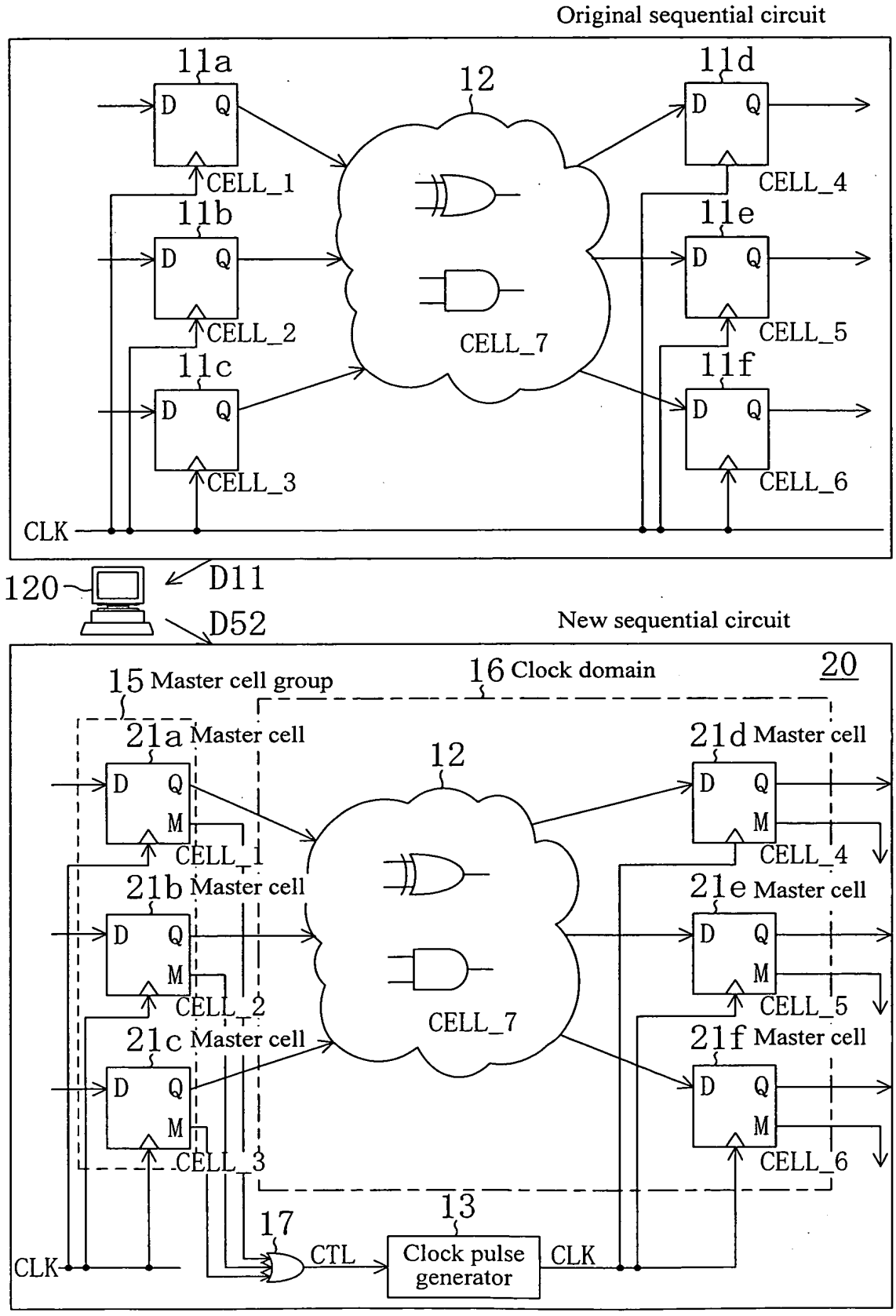
Original sequential circuit
11a
12
11d
D Q
CELL_1
CELL_4
11b
11e
CELL_2
CELL_7
CELL_5
11c
11f
CELL_3
CELL_6
CLK
120
D11
D52
New sequential circuit
15 Master cell group
16 Clock domain
20
21a Master cell
21d Master cell
M
21b Master cell
21e Master cell
21c Master cell
21f Master cell
13
17
CTL
Clock pulse generator

FIG. 24

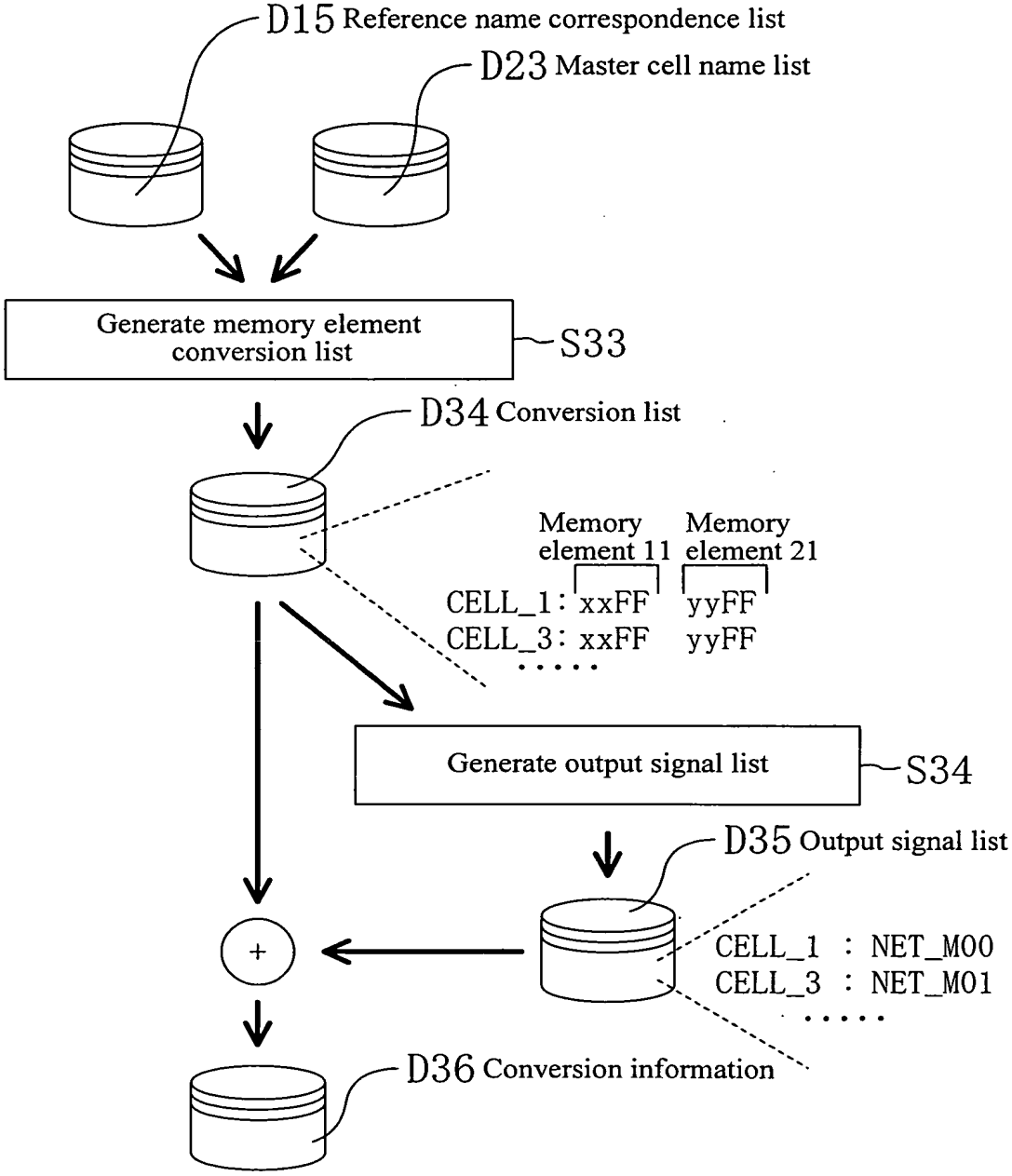
D15 Reference name correspondence list
D23 Master cell name list
Generate memory element conversion list
S33
D34 Conversion list
Memory element 11
Memory element 21
CELL_1: xxFF yyFF
CELL_3: xxFF yyFF
Generate output signal list
S34
D35 Output signal list
CELL_1 : NET_M00
CELL_3 : NET_M01
+
D36 Conversion information

FIG. 25

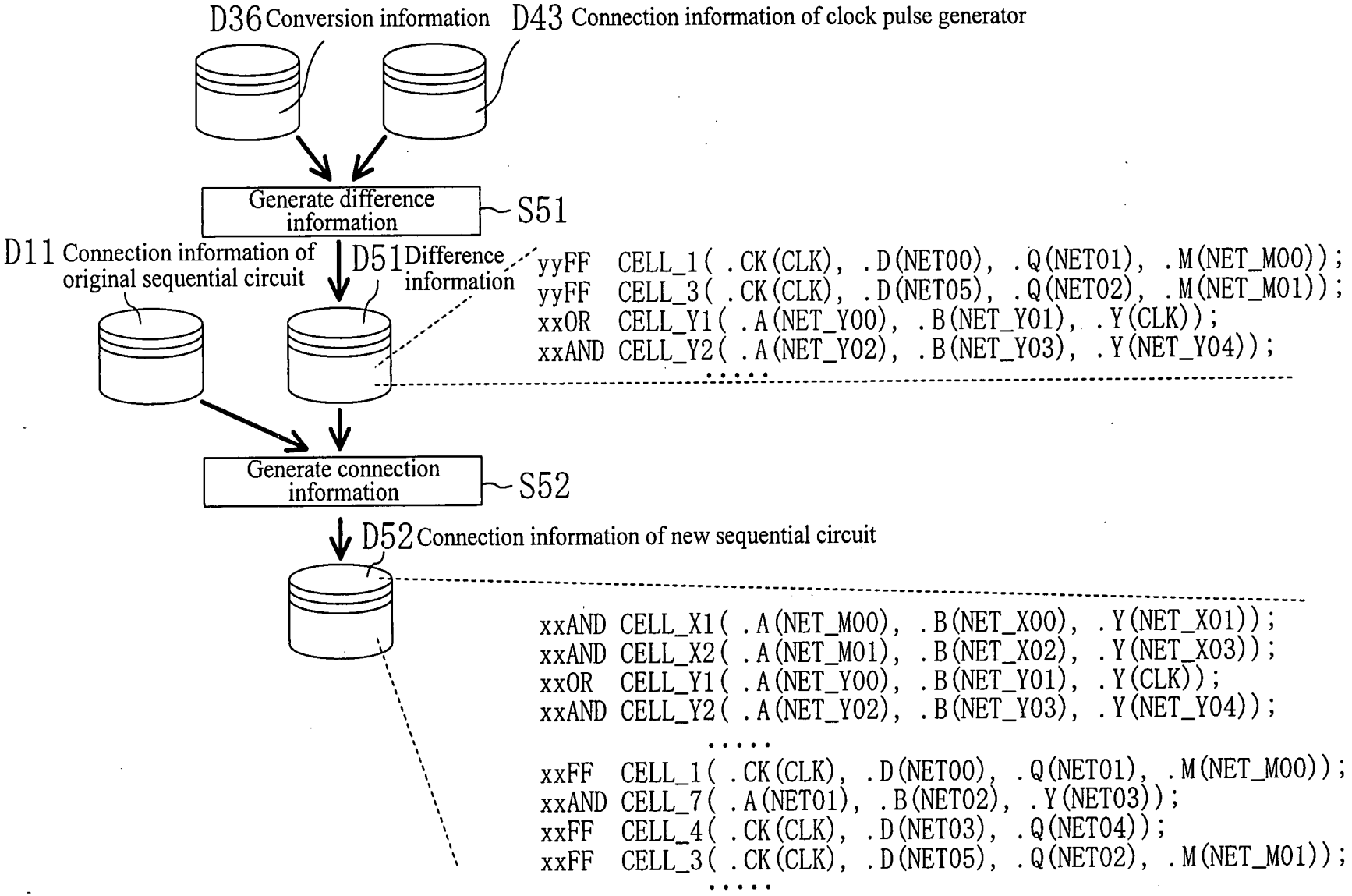
D36 Conversion information
D43 Connection information of clock pulse generator
Generate difference information
S51
D11 Connection information of original sequential circuit
D51 Difference information
yyFF CELL_1(.CK(CLK), .D(NET00), .Q(NET01), .M(NET_M00));
yyFF CELL_3(.CK(CLK), .D(NET05), .Q(NET02), .M(NET_M01));
xxOR CELL_Y1(.A(NET_Y00), .B(NET_Y01), .Y(CLK));
xxAND CELL_Y2(.A(NET_Y02), .B(NET_Y03), .Y(NET_Y04));
.....
Generate connection information
S52
D52 Connection information of new sequential circuit
xxAND CELL_X1(.A(NET_M00), .B(NET_X00), .Y(NET_X01));
xxAND CELL_X2(.A(NET_M01), .B(NET_X02), .Y(NET_X03));
xxOR CELL_Y1(.A(NET_Y00), .B(NET_Y01), .Y(CLK));
xxAND CELL_Y2(.A(NET_Y02), .B(NET_Y03), .Y(NET_Y04));
.....
xxFF CELL_1(.CK(CLK), .D(NET00), .Q(NET01), .M(NET_M00));
xxAND CELL_7(.A(NET01), .B(NET02), .Y(NET03));
xxFF CELL_4(.CK(CLK), .D(NET03), .Q(NET04));
xxFF CELL_3(.CK(CLK), .D(NET05), .Q(NET02), .M(NET_M01));
.....

FIG. 26

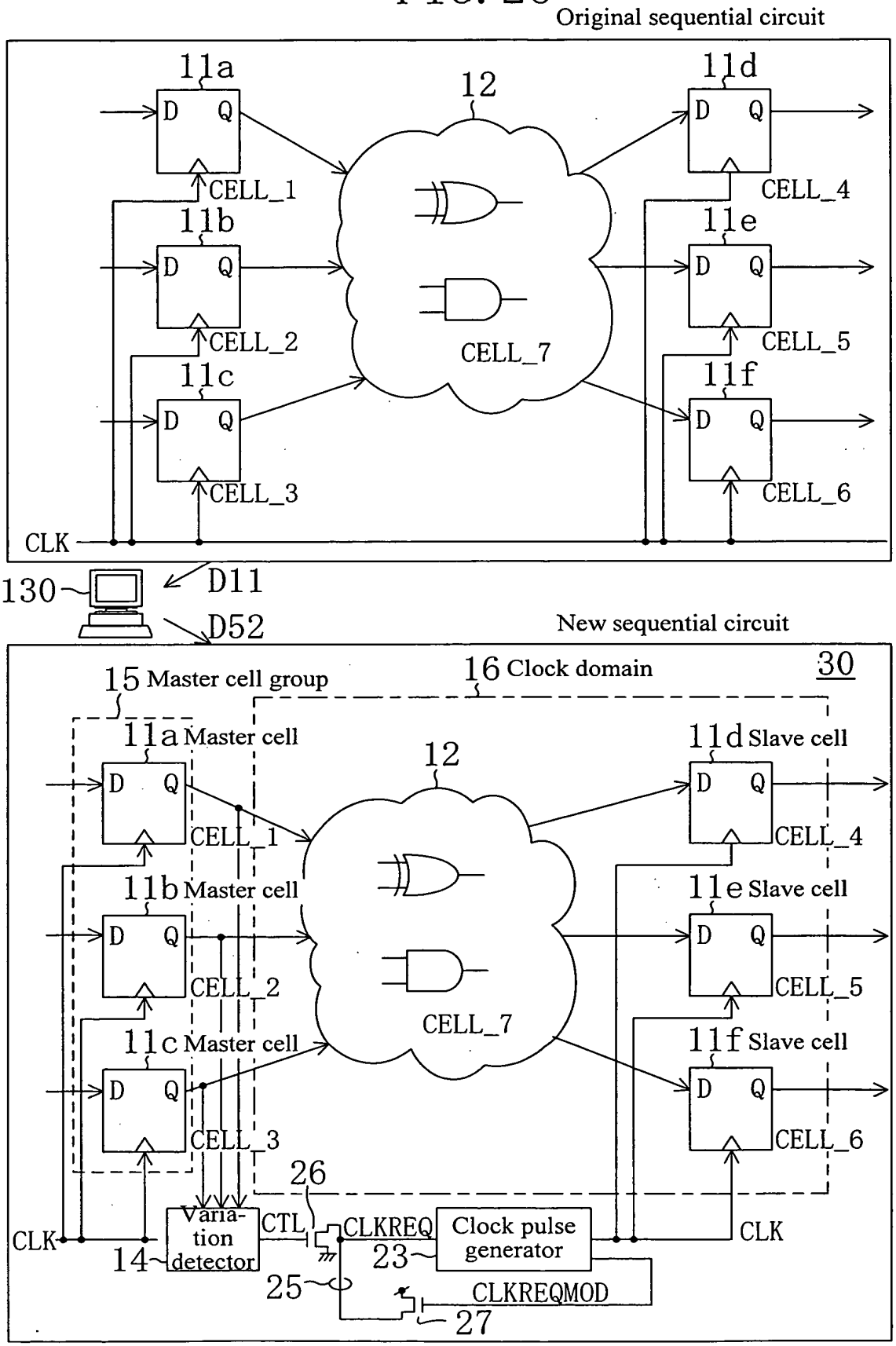
Original sequential circuit
11a
12
11d
D Q
CELL_1
CELL_4
11b
11e
CELL_2
CELL_7
CELL_5
11c
11f
CELL_3
CELL_6
CLK
130
D11
D52
New sequential circuit
15 Master cell group
16 Clock domain
30
11a Master cell
11d Slave cell
11b Master cell
11e Slave cell
11c Master cell
11f Slave cell
26
Varia-
tion
detector
CTL
CLKREQ
Clock pulse
generator
14
23
25
CLKREQMOD
27

FIG. 27

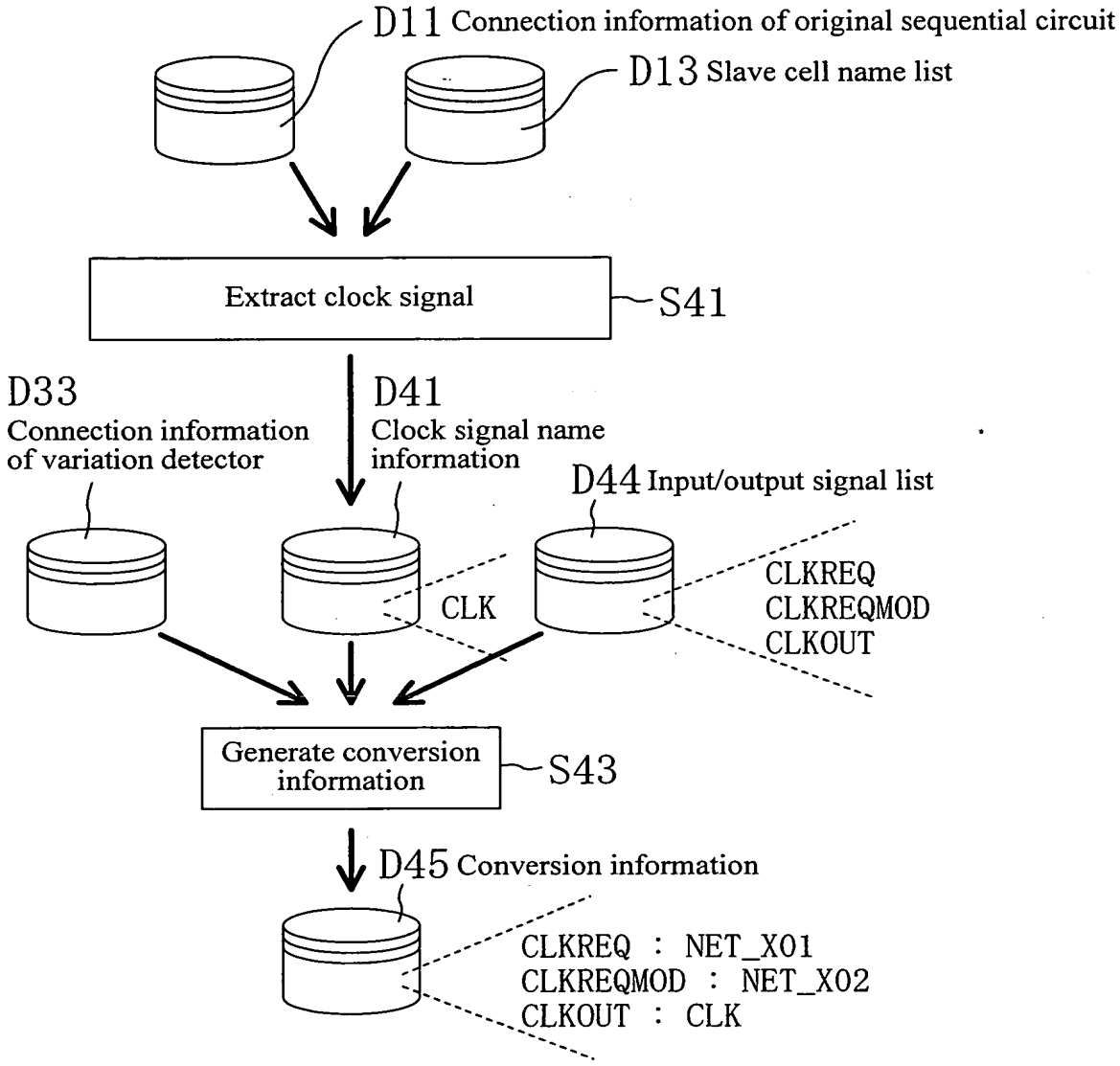
D11 Connection information of original sequential circuit
D13 Slave cell name list
Extract clock signal
S41
D33
Connection information of variation detector
D41
Clock signal name information
D44 Input/output signal list
CLK
CLKREQ
CLKREQMOD
CLKOUT
Generate conversion information
S43
D45 Conversion information
CLKREQ : NET_X01
CLKREQMOD : NET_X02
CLKOUT : CLK

FIG. 28

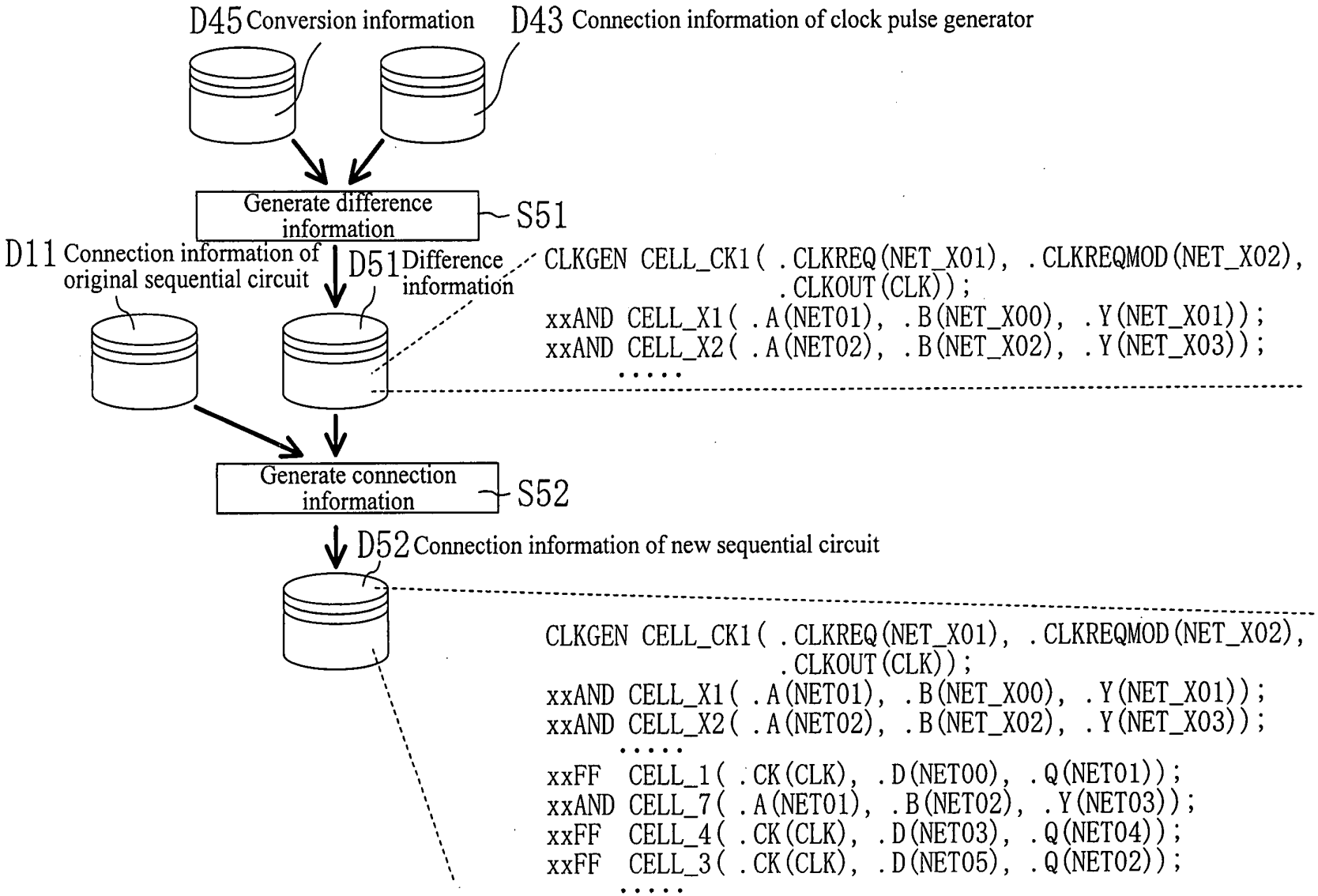
D45 Conversion information
D43 Connection information of clock pulse generator
Generate difference information
S51
D11 Connection information of original sequential circuit
D51 Difference information
CLKGEN CELL_CK1(.CLKREQ(NET_X01), .CLKREQMOD(NET_X02),
.CLKOUT(CLK));
xxAND CELL_X1(.A(NET01), .B(NET_X00), .Y(NET_X01));
xxAND CELL_X2(.A(NET02), .B(NET_X02), .Y(NET_X03));
.....
Generate connection information
S52
D52 Connection information of new sequential circuit
CLKGEN CELL_CK1(.CLKREQ(NET_X01), .CLKREQMOD(NET_X02),
.CLKOUT(CLK));
xxAND CELL_X1(.A(NET01), .B(NET_X00), .Y(NET_X01));
xxAND CELL_X2(.A(NET02), .B(NET_X02), .Y(NET_X03));
.....
xxFF CELL_1(.CK(CLK), .D(NET00), .Q(NET01));
xxAND CELL_7(.A(NET01), .B(NET02), .Y(NET03));
xxFF CELL_4(.CK(CLK), .D(NET03), .Q(NET04));
xxFF CELL_3(.CK(CLK), .D(NET05), .Q(NET02));
.....

FIG. 29

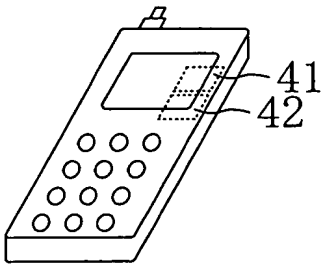

FIG. 30

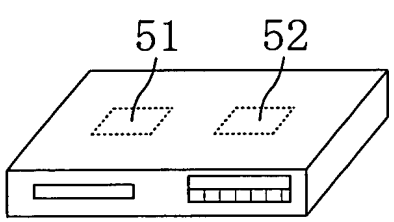

FIG. 31

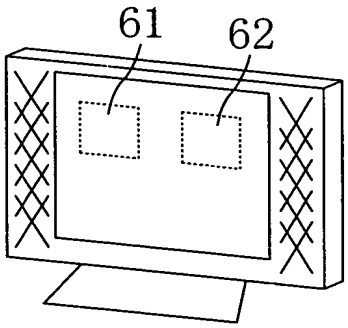

FIG. 32

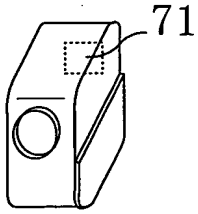

FIG. 33

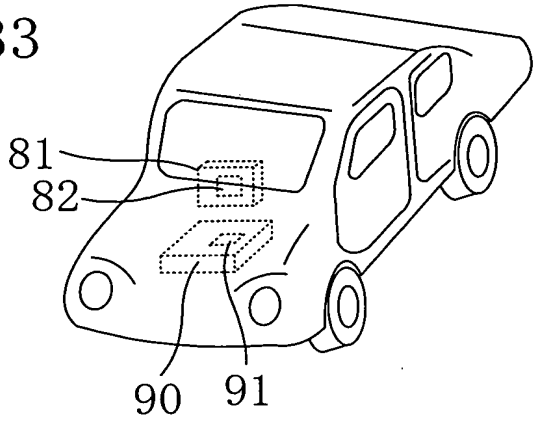

FIG. 34A

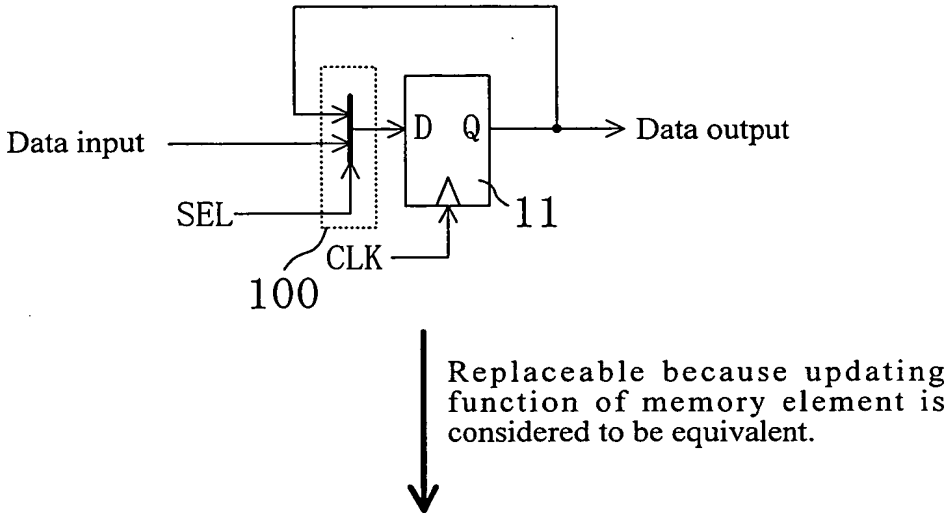

FIG. 34B

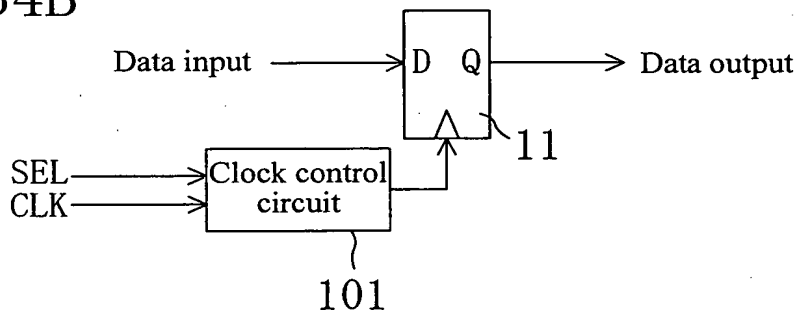

FIG. 35A

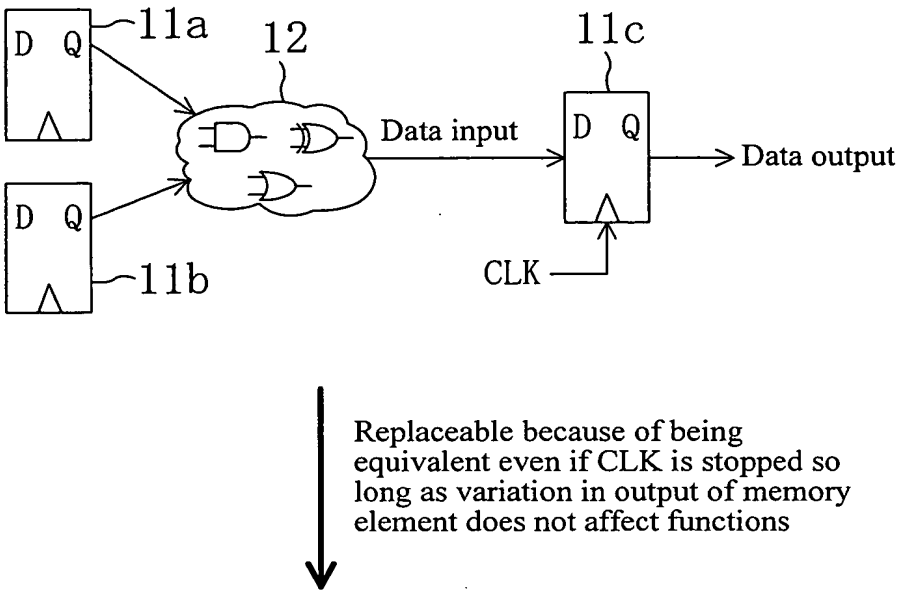

FIG. 35B